Application Note

# Poly-Phase Energy Metering IC

## M90E36A

## APPLICATION OUTLINE

This document describes system application issues when using the M90E36A (poly-phase energy metering ICs) to design poly-phase energy meters.

The M90E36A is applicable in class 0.5S or class 1 poly-phase meter design and also supports three-phase four-wire (3P4W, Y0) or three-phase three-wire (3P3W, Y or Δ) connection modes. The M90E36A can also be used in harmonic meter design.

The M90E36A uses 3.3V single power supply. In a typical 3P4W design, there are three transformers&regulators to provide power supply. The AC power supply outputs 3.3V to chip digital power supply DVDD after rectifier and voltage regulation. The analog power supply AVDD should be connected directly to digital power supply DVDD.

The M90E36A has on-chip power-on-reset circuit. The $\overline{\text{RESET}}$ pin should be connected to DVDD through a 10kΩ resistor and a 0.1μF filter capacitor to ground. The M90E36A has highly stable on-chip reference power supply. The Vref pin should be decoupled with a 10μF capacitor and a 0.1μF ceramic capacitor.

The M90E36A employs 16.384MHz as the system frequency. The M90E36A has built-in crystal oscillator circuit and 10pF matching capacitance. Users only need to connect a 16.384MHz crystal between OSCI and OSCO pins in application.

The M90E36A provides a 4-wire SPI interface ($\overline{\text{CS}}$, SCLK, SDI and SDO) for external MCU connection. MCU can perform chip configuration and register reading/writing through SPI. The M90E36A also supports Master mode SPI, which is named Direct Memory Access (DMA) mode. In DMA mode, The M90E36A streams out ADC sampling raw data to external MCU at an up to 1800kbps rate.

The M90E36A provides four energy pulse output pins: active energy pulse CF1, reactive energy pulse CF2 (can also be configured as apparent energy pulse), fundamental energy pulse CF3 and harmonic energy pulse CF4. They can be used for energy metering calibration and can also be connected to MCU for energy accumulation.

The M90E36A provides three zero-crossing pins ZX0, ZX1 and ZX2 which can select different phase's voltage or current as inputs.

The M90E36A provides three output pins IRQ0, IRQ1 and WarnOut to generate interrupt and warn out signals at different levels.

The default application in this document is 3P4W, otherwise it will be specially indicated.

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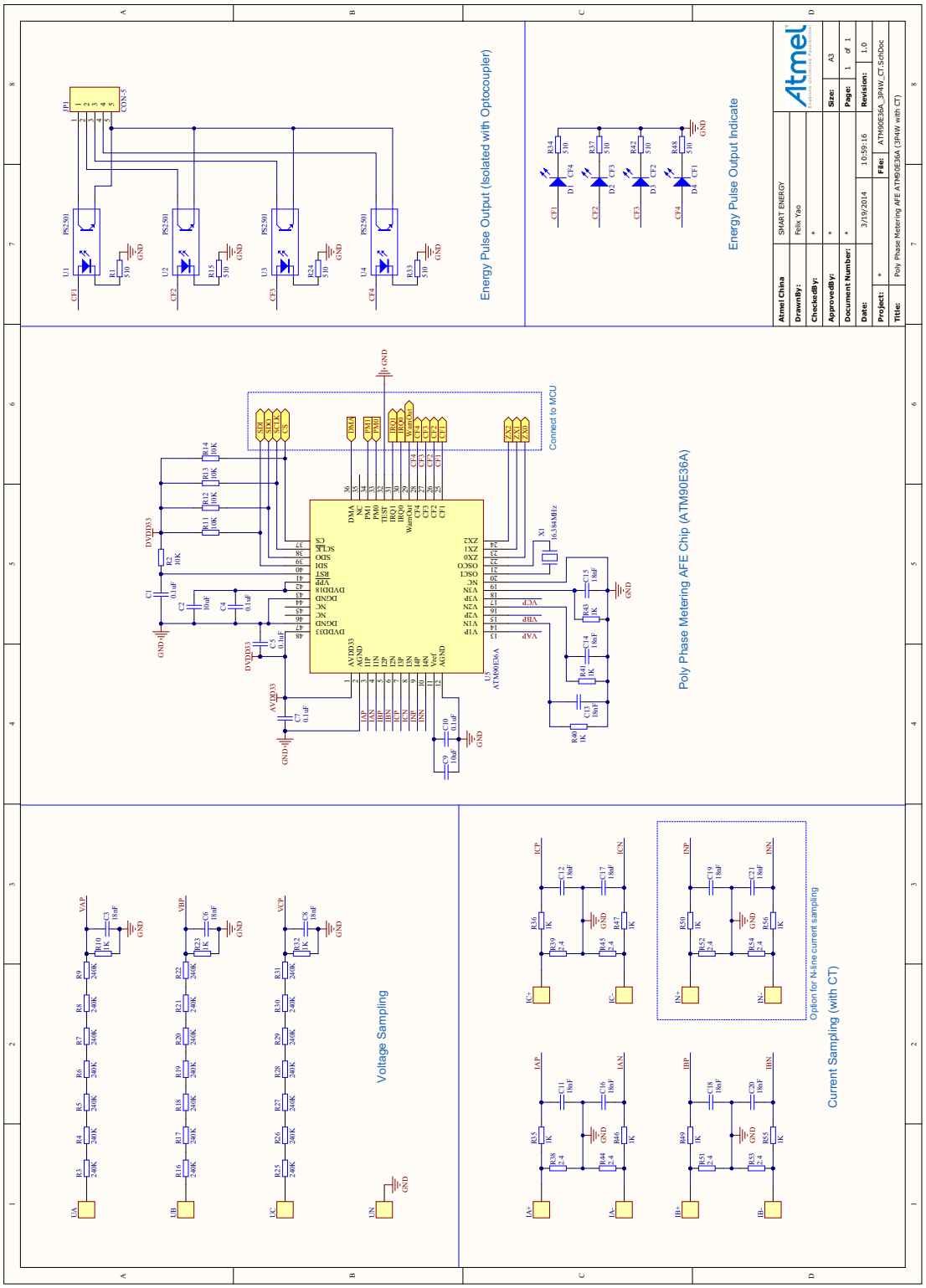
# 1 HARDWARE REFERENCE DESIGN

## 1.1 3P4W APPLICATION

### 1.1.1 Schematics (Current Transformer (CT))

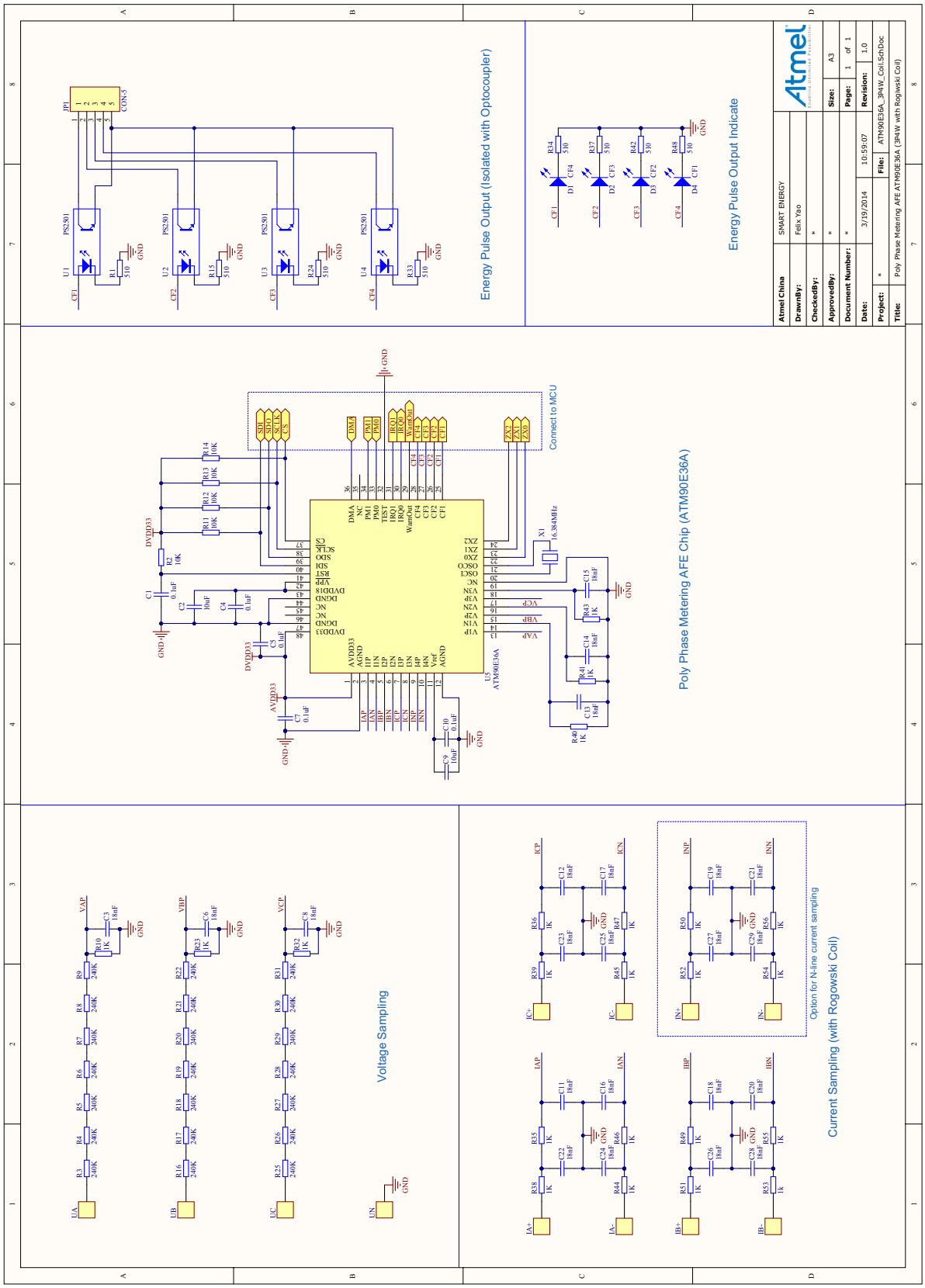


### 1.1.2 BOM (CT)

**Table-1 3P4W BOM (CT)**

| Component Type | Designator | Quantity | Parameter | Tolerance |
|---|---|---|---|---|
| SMT Capacitor | C3 C6 C8 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 | 14 | 18nF | ±10% X7R (anti-aliasing filter capacitor) |
| | C1 C4 C5 C7 C10 | 5 | 0.1μF | ±10% X7R |
| | C2 C9 | 2 | 10μF | ±10% X7R |
| SMT Resistor | R38 R39 R44 R45 R51 R52 R53 R54 | 8 | 2.4Ω | ±1% 1/8W 25ppm |
| | R1 R15 R24 R33 R34 R37 R42 R48 | 8 | 510Ω | ±5% 1/8W 100ppm |
| | R10 R23 R32 R35 R36 R40 R41 R43 R46 R47 R49 R50 R55 R56 | 14 | 1kΩ | ±1% 1/8W 25ppm (anti-aliasing filter resistor) |
| | R2 R11 R12 R13 R14 | 5 | 10kΩ | ±5% 1/8W 100ppm |
| | R3~R9, R16~R22, R25~R31 | 21 | 240kΩ | ±1% 1/8W 25ppm |
| LED | D1 D2 D3 D4 | 4 | - | - |
| SMT Optocoupler | U1 U2 U3 U4 | 4 | PS2501 | - |
| Crystal | X1 | 1 | 16.384MHz | ±20ppm |
| IC | U5 | 1 | M90E36A | - |
| Connector | JP1 | 1 | CON-5 | - |

### 1.1.3 Schematics (Rogowski)



### 1.1.4 BOM (Rogowski)

**Table-2 3P4W BOM (Rogowski)**

| Component Type | Designator | Quantity | Parameter | Tolerance |
|---|---|---|---|---|
| SMT Capacitor | C3 C6 C8 C11 C12 C13 C14 C15 C16 C17 C18 C19 C20 C21 C22 C23 C24 C25 C26 C27 C28 C29 | 22 | 18nF | ±10% X7R (anti-aliasing filter capacitor) |
| | C1 C4 C5 C7 C10 | 5 | 0.1μF | ±10% X7R |
| | C2 C9 | 2 | 10μF | ±10% X7R |
| SMT Resistor | R1 R15 R24 R33 R34 R37 R42 R48 | 8 | 510Ω | ±5% 1/8W 100ppm |
| | R10 R23 R32 R35 R36 R38 R39 R40 R41 R43 R44 R45 R46 R47 R49 R50 R51 R52 R53 R54 R55 R56 | 14 | 1kΩ | ±1% 1/8W 25ppm (anti-aliasing filter resistor) |
| | R2 R11 R12 R13 R14 | 5 | 10kΩ | ±5% 1/8W 100ppm |
| | R3~R9, R16~R22, R25~R31 | 21 | 240kΩ | ±1% 1/8W 25ppm |
| LED | D1 D2 D3 D4 | 4 | - | - |
| SMT Optocoupler | U1 U2 U3 U4 | 4 | PS2501 | - |
| Crystal | X1 | 1 | 16.384MHz | ±20ppm |
| IC | U5 | 1 | M90E36A | - |
| Connector | JP1 | 1 | CON-5 | - |

### 1.1.5 Circuit Description

The recommended circuit for the M90E36A three-phase four-wire (3P4W) application is as shown in 1.1.1 Schematics (Current Transformer (CT)). The M90E36A can use CT and Rogowski coil in current sampling. The recommended circuit for 3P4W application with Rogowski coil is as shown in 1.1.3 Schematics (Rogowski).

It is recommended to use two-order filtering when sampling with Rogowski coil. The other parts are the same as the CT application circuit. The recommended type of Rogowski coil is: PA3202NL (Pulse Electronics).

Poly-phase voltage is sampled over resistor divider network with recommended ratio of 240KΩ x 7:1KΩ. The anti-aliasing filter capacitor is recommended to be 18nF. Poly-phase current and N line current are sampled over CT. The CT ratio and load resistance should be selected based on the actual metering range. The anti-aliasing filter resistance/capacitor is suggested to be 1KΩ/18nF for the current sampling circuit.

The CF1~CF4 pins are provided with driving capacity of 8mA which can drive LED and optocoupler parallelly. The other digital pins are provided with driving capacity of 3mA which can drive optocoupler directly.

*Application note: how to select CT and CT load resistance*

Condition:

M90E36A ADC input voltage range is 120μVrms ~ 720mVrms

M90E36A ADC input gain PGA_GAIN = 1, 2, 4

Assume:

Metering range of the energy meter is Imin ~ Imax

CT current output ratio is N:1

CT load resistance is $R_{CT}$

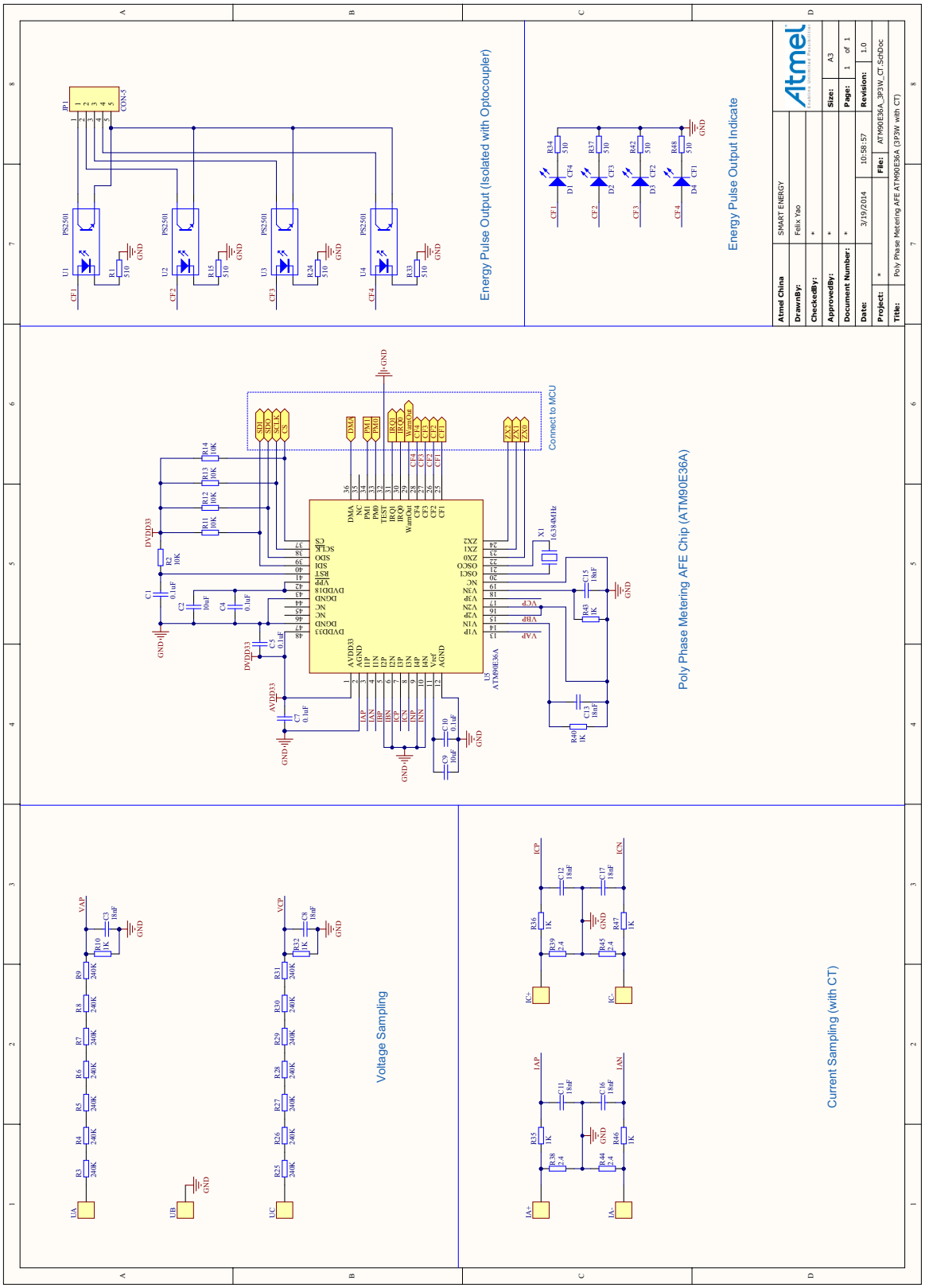
So the parameters meet the formula as below:

$$120\mu Vrms < \frac{PGA\_GAIN \times R_{CT} \times I_{min}}{N}$$

$$\frac{PGA\_GAIN \times R_{CT} \times I_{max}}{N} < 720mVrms$$

## 1.2 3P3W APPLICATION

### 1.2.1 Schematics



### 1.2.2 BOM

**Table-3 3P3W BOM**

| Component Type | Designator | Quantity | Parameter | Tolerance |
|---|---|---|---|---|
| SMT Capacitor | C3 C8 C11 C12 C13 C15 C16 C17 | 8 | 18nF | ±10% X7R (anti-aliasing filter capacitor) |
| | C1 C4 C5 C7 C10 | 5 | 0.1μF | ±10% X7R |
| | C2 C9 | 2 | 10μF | ±10% X7R |
| SMT Resistor | R38 R39 R44 R45 | 4 | 2.4Ω | ±1% 1/8W 25ppm |
| | R1 R15 R24 R33 R34 R37 R42 R48 | 8 | 510Ω | ±5% 1/8W 100ppm |
| | R10 R32 R35 R36 R40 R43 R46 R47 | 8 | 1kΩ | ±1% 1/8W 25ppm (anti-aliasing filter resistor) |
| | R2 R11 R12 R13 R14 | 5 | 10kΩ | ±5% 1/8W 100ppm |
| | R3~R9, R25~R31 | 14 | 240kΩ | ±1% 1/8W 25ppm |
| LED | D1 D2 D3 D4 | 4 | - | - |
| SMT Optocoupler | U1 U2 U3 U4 | 4 | NEC2501 | - |
| Crystal | X1 | 1 | 16.384MHz | ±20ppm |
| IC | U5 | 1 | M90E36A | - |
| Connector | JP1 | 1 | CON-5 | - |

### 1.2.3 Circuit Description

This circuit is the recommended circuit for the M90E36A three-phase three-wire (3P3W) application.

Phase B is the reference ground in 3P3W application. In 3P3W system, Uab stands for Ua, Ucb stands for Uc and there is no Ub.

Phase B voltage, phase B current and N line sampling current are not needed in 3P3W application. Pin 5, 6, 9, 10, 15 and 16 should be connected to GND.

If DMA function is not used, pin 36 should also be connected to GND. All NC pins should be left open.

The other parts of 3P3W application circuit are similar to 3P4W and can be treated in the same way.

# 2 INTERFACE

The M90E36A provides a four-wire SPI interface (CS, SCLK, SDI and SDO). The interface can be configured to two modes by the DMA_CTRL pin: Slave mode and Master mode.

## 2.1 SPI

The SPI interface in Slave mode is mainly used for register read/write operation. A complete SPI read/write operation is of 32 bits, which contains 16-bit address and 16-bit data. In the 16-bit address, bit0 ~ bit9 correspond to valid register address A0 ~ A9, and bit10 ~ bit14 are reserved (these bits are don't-care). Bit15 indicates the SPI operation is read or write.

| SPI Operation | Description | Highest Bit (Bit15) |
|---|---|---|
| Read | Read register data | 1 |
| Write | Write data to register | 0 |

The transmission of address and data bits is from high to low, which means MSB first and LSB last. Note that the M90E36A read/write only supports single address operation, rather than continuous read or write.

The M90E36A has a special register LastSPIData [0FH] for recording the last SPI read/write data. This register can be used for data check for SPI read/write operation. When the system is in strong interference situation, the disturbance signal may cause SPI communication disorder and result in SPI read/write error. In this case, LastSPIData can be used to check the correctness of SPI read/write and strengthen system robustness. For read-clear registers, if the read data is different from the LastSPIData data, the actual data can be obtained by reading the LastSPIData register repeatedly.

LastSPIData application is as shown in Figure-1 and Figure-2:

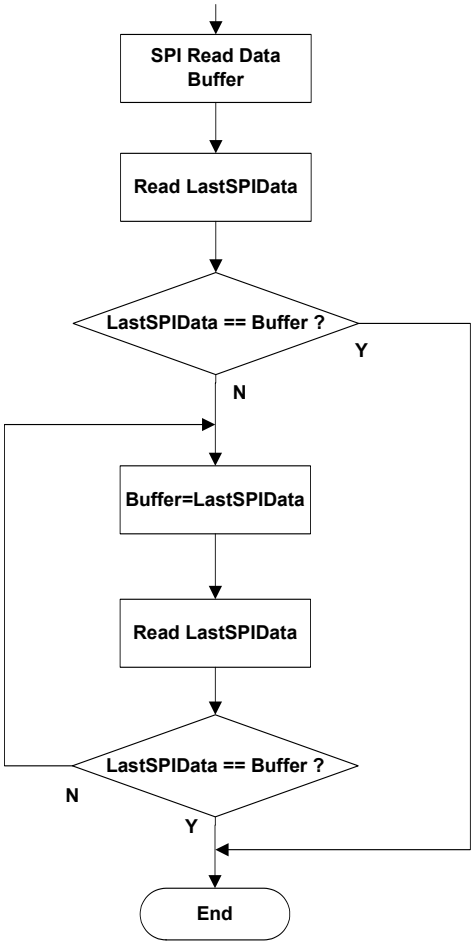



***Figure-1 LastSPIData Application (Read)***

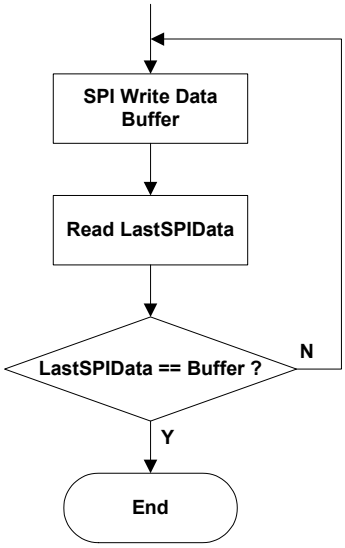



*Figure-2 LastSPIData Application (Write)*

## 2.2 DMA

For details please refer to the “SPI/DMA Interface” chapter in the M90E36A datasheet.

# 3 POWER MODES

Four power modes are supported which correspond to four kinds of power consumption. The power mode is configured by PM1/PM0 pins.

| PM1 | PM0 | Power Modes | Power Consumption |
|---|---|---|---|
| 1 | 1 | Normal mode | High ↓ Low |
| 1 | 0 | Partial Measurement mode | |
| 0 | 1 | Detection mode | |
| 0 | 0 | Idle mode | |

## 3.1 NORMAL MODE

In Normal mode, all function blocks are active except for the current detector block. All registers can be accessed, including the registers related to Partial Measurement mode and Detection mode.

## 3.2 PARTIAL MEASUREMENT MODE

In Partial Measurement mode, only three-phase current sampling and the related blocks are active. SPI communication is normal in this mode, but only partial measurement related registers and some special registers can be accessed by external MCU.The accessible registers in Partial Measurement mode are listed as below:

| Address | Name | Address | Name | Address | Name |
|---|---|---|---|---|---|
| 00H | SoftReset | 14H | PMOffsetA | 1AH | PMIrmsC |
| 01H | SysStatus0 | 15H | PMOffsetB | 1BH | PMConfig |
| 03H | FuncEn0 | 16H | PMOffsetC | 1CH | PMAvgSamples |
| 07H | ZXConfig | 17H | PMPGA | 1DH | PMIrmsLSB |
| 0EH | DMACtrl | 18H | PMIrmsA | | |
| 0FH | LastSPIData | 19H | PMIrmsB | | |

There is a special enable control bit ReMeasure (bit14 of PMConfig) for Partial Measurement mode. When the control bit is enabled, sampling and measurement are proceeded at the sampling period determined by the PMAvgSamples[1CH] register.

Measure function is automatically shut off upon measurement completion. It needs to be enabled again if to measure again. Upon measurement completion, the IRQ0 pin outputs high level. MCU can judge whether measurement is completed through IRQ0. IRQ0 is cleared when the control bit (ReMeasure) is enabled again or partial measurement mode is exited.

There is also a special “Busy” indication bit PMBusy (bit0 of PMConfig) for Partial Measurement mode. MCU can also judge whether measurement is completed through the PMBusy bit.

Accuracy of current measurement in Partial Measurement mode is the same as Normal mode, because reference power supply module is active.

## 3.3 DETECTION MODE

In Detection mode, only the current detector is active and all the registers can not be accessed by external MCU. In this mode, each I/O is in specific state (for details refer to datasheet) and SPI is disabled. So the control and threshold registers for Detection mode need to be programmed in Normal mode before entering Detection mode. Once these related registers are written, there is no need to re-configure them when switching between different power modes. Detection mode related registers are listed as below:

| Address | Name |
|---|---|
| 10H | DetectCtrl |
| 11H | DetectThA |
| 12H | DetectThB |
| 13H | DetectThC |

Current detection is achieved with low power comparators. Two comparators are supplied for each phase on detecting positive and negative current. When any single-phase current or multiple-phase current exceeds the configured threshold, the IRQ0 pin is asserted high. When all three phase currents exceed the configured threshold, the IRQ1 pin is asserted high. The IRQ0/IRQ1 state is cleared when entering or exiting Detection mode.

The all three phase currents are considered as the currents of three current channels I1~I3. As there is no phase B current in 3P3W application, IRQ1 will not be asserted high even if both phase A and phase C current exceed the configured threshold.

## 3.4 IDLE MODE

In Idle mode, all the modules are disabled and all the registers can not be accessed. In this mode, each I/O is in a specific state (for details refer to datasheet) and SPI is disabled. All register values are lost except for current detection related registers.

## 3.5 TRANSITION AND APPLICATION OF POWER MODES

The four power modes are controlled by the PM0 and PM1 pins. In application, any power mode transition goes through Idle mode to avoid register value confusion or system status uncertainty in mode transition. All function modules are disabled in Idle mode while the related modules will be enabled after switching from Idle mode to other mode, which is equivalent to reset to the function modules, thus ensuring normal operation of the function modules.

It needs to reload registers to ensure normal operation when switching from Idle mode to Normal mode or Partial Measurement mode, while no need to reload registers when switching from Idle mode to Detection mode. Power mode transition is shown as Figure-3:

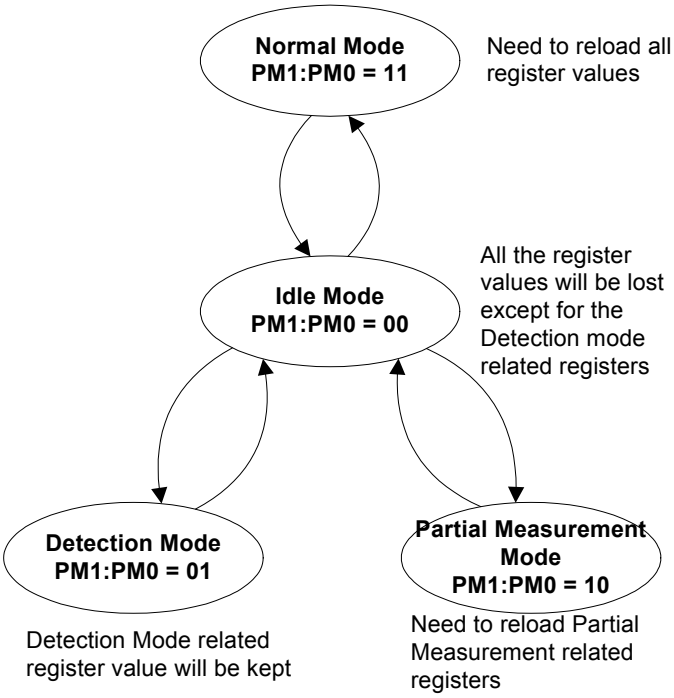



***Figure-3 Power Mode Transition***

Note: For description convenience, the intermediary Idle mode will be omitted when refering to power mode transition.

The most typical application of power mode transition is no-voltage detection for power meter.

The so-called no-voltage state is when all phase voltages are less than the voltage threshold but the load current is greater than the configured current value (such as 5% of rated current). In no-voltage state, the power meter usually uses backup battery for power supply. The system needs to enter low power mode and perform measurement and recording for no-voltage state periodically.

The recommended flow for power meter with the M90E36A is as below:

1 Set the current detection threshold to be the minimum load current (such as 5% of rated current) required in no-voltage state.
2 When no-voltage happens, the system enters Idle mode;
3 The system enters Detection mode every once in a while (such as 5s);
4 Once the load current is greater than the configured value, the system enters Partial Measurement mode to measure and record the load current;
5 The system returns to Idle mode after measurement and recording are completed;
6 The system enters Partial Measurement mode every once in a while (such as 60s) to measure and record the load current.

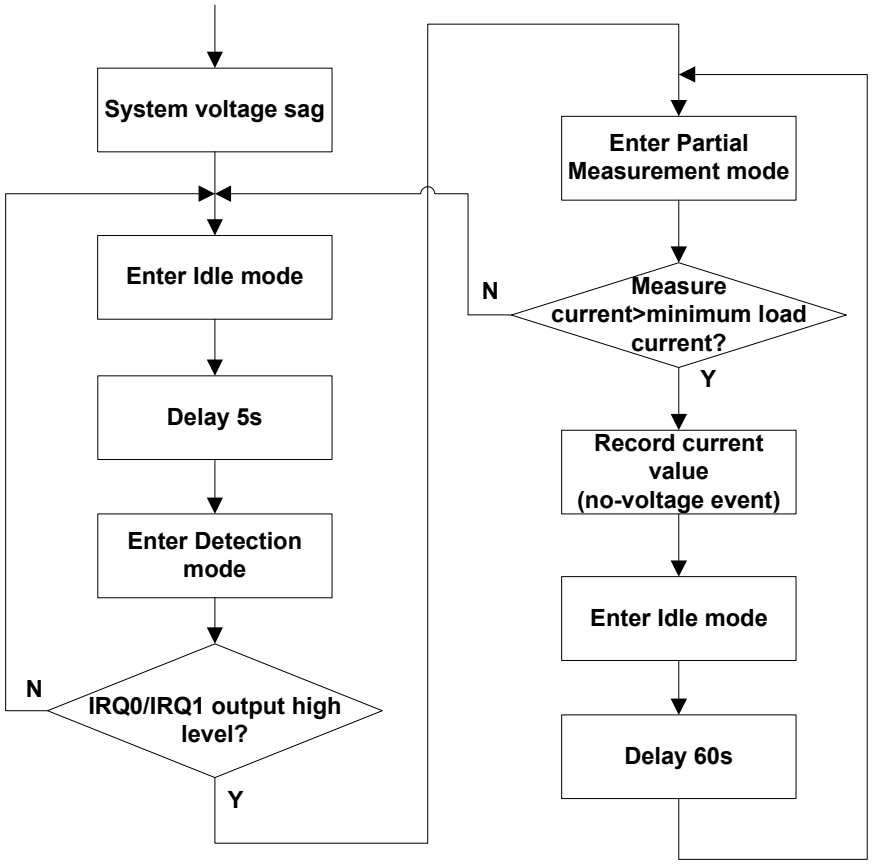



***Figure-4 Application of Detection Mode and Partial Measurement Mode***

*Application note: Design principle for current detection threshold*

It is recommended to do system design based on current detection threshold of 3mVrms.

Example:

Assume:

The requirement is that the minimum load current detected is 5% of rated current. Current specification is 5(60)A;

The minimum load current is Id, which corresponds to a 3mVrms ADC input signal.

The parameters meet the following relations:

| | **Minimum Detection Load Current Id** | **Rated Current In** | **Maximum Current Imax** |
|---|---|---|---|
| ratio to rated current | 5% In | In | 12In |
| corresponding ADC input signal | 3mVrms | 60mVrms | 720mVrms |
| actual current | 250mA | 5A | 60A |

# 4 CALIBRATION

## 4.1 CALIBRATION METHOD

Normally voltage, current, mean power, phase angle, frequency and so on are regarded as measurement values, while active energy, reactive energy and so on are regarded as metering value.

Measurement and metering function both need calibration before normal use as shown in below table:

| Power Mode | Parameter | Need Calibration | Calibration Method |
|---|---|---|---|
| Normal mode | voltage/current | √ | offset/gain calibration |
| | power/frequency/phase angle/ power factor | X | -- |
| | THD | X | -- |
| | full-wave energy metering | √ | offset/gain/phase angle calibration |
| | fundamental energy metering | √ | offset/gain calibration |
| | harmonic energy metering | X | -- |
| Partial Measurement mode | current measurement | √ | offset/gain calibration |
| Detection mode | current detection | √ | threshold calibration |

In typical application of three-phase power meter, voltage, current and full-wave energy must be calibrated. The others can be calibrated according to actual application, no need to calibrate if no use.

The calibration flow follows the sequence of measurement first then metering. Metering calibration is realized by first calibrating gain and then calibrating phase angle compensation, only single-point calibration is needed over the entire dynamic range. Reactive does not need to be calibrated since it is guaranteed by chip design.

Frequency, phase angle and power factor do not need calibration, since their accuracy is guaranteed by chip design.

## 4.2 CALIBRATION IN NORMAL MODE

The basic functions, such as measurement, metering, harmonic analysis and so on are only active in Normal mode. So calibration in Normal mode is basic and a must. The related registers need to be configured before calibration. Calibration flow is as shown in Figure-5.

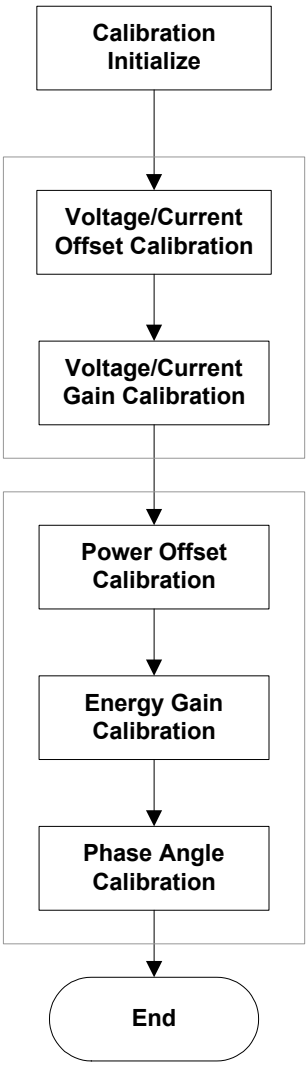



*Figure-5 Active Energy Metering Calibration Flow in Normal Mode*

### 4.2.1 Measurement/Metering Startup Command (Configstart/Calstart/HarmStart/AdjStart)

Startup command registers have multiple valid settings for different operation modes.

| Startup Register Value | Usage | Operation |
|---|---|---|
| 6886H | Rower up state | It is the value after reset. This state blocks checksum checking error generation |
| 5678H | Calibration | Similar like 6886H, This state blocks checksum checking error generation. Writing with this value trigger a reset to the associated registers. |
| 8765H | Operation | Checksum checking is enabled and if error detected, IRQ/Warn is asserted and Metering stopped. |
| Other | Error | Force checksum error generation and system stop. |

The default value for these registers is '6886H' after power-on reset. At this time, measurement functions can be started but metering functions can not. The measurement/ metering functions will be started when related startup registers are set to '5678H' or '8765H'. If other values are written to these registers, the corresponding measurement/ metering functions will be disabled, the corresponding checksum and CSxErr bits will be set and the WarnOut pin will output high level.

| Startup Register/ Address | Register Address Range (CSx Calculation Range) | Register Function | CSx / Address | Function Startup on Reset |
|---|---|---|---|---|
| ConfigStart / 30H | 31H ~ 3AH | function configuration | CS0 / 3BH | -- |
| CalStart / 40H | 41H ~ 4CH | energy metering calibration | CS1 / 4DH | not startup |
| HarmStart / 50H | 51H ~ 56H | fundamental/ harmonic energy metering calibration | CS2 / 57H | not startup |
| AdjStart / 60H | 61H ~ 6EH | measurement value calibration | CS3 / 6FH | startup |

When '5678H' is written, the registers resume to their power-on values and metering/measurement functions are started without checksum check.

When '8765H' is written, the registers do not resume to their power-on values, but checksum will be checked. If the written checksum is the same as the system self generated checksum, normal metering/measurement functions will be started. If they are different, metering/measurement functions will not be started, the corresponding CSxErr bits are set and the WarnOut pin outputs high level. Note that if CS2 is not correct, when the startup register (xxxStart) is 8765H, only harmonic measurement and metering functions will be disabled. But if CS0, CS1 or CS3 are not correct, all measurement and metering functions will be disabled.

The written checksum means the value MCU (or other external processor) writes to the addresses 3BH/4DH/57H/6FH through SPI. The value acquired by MCU reading through SPI is the checksum generated internally. When the startup register (xxxStart) is 5678H or 8765H, the M90E36A will calculate checksum automatically. As long as there is any register change, the corresponding CSx value will be updated immediately. So in application the MCU process can be simplified by reading the CSx registers first to get the correct checksum, then writing the checksum directly back to the CSx registers.

| Address | Name | Bit15 ~ Bit0 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 01H | SysStatus0 | Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit9 | Bit8 |
| | | - | CS0Err | - | CS1Err | - | CS2Err | - | CS3Err |
| | | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| | | URevWn | IRevWn | - | - | SagWarn | PhaseLoseWn | - | - |

1 CS0Err: indicates CS0 checksum status
0: CS0 checksum correct (default)
1: CS0 checksum error. The WarnOut pin is asserted at the same time.

2 CS1Err: indicates CS1 checksum status
0: CS1 checksum correct (default)
1: CS1 checksum error. The WarnOut pin is asserted at the same time.

3 CS2Err: indicates CS2 checksum status
0: CS2 checksum correct (default)
1: CS2 checksum error. The WarnOut pin is asserted at the same time.

4 CS3Err: indicates CS3 checksum status
0: CS3 checksum correct (default)
1: CS3 checksum error. The WarnOut pin is asserted at the same time.

In application, it is recommended to set all the startup registers (xxxStart) to 8765H, and timely check the startup registers (xxxStart) and checksum status indicate bits (CSxErr) in order to judge whether system is in normal operation.

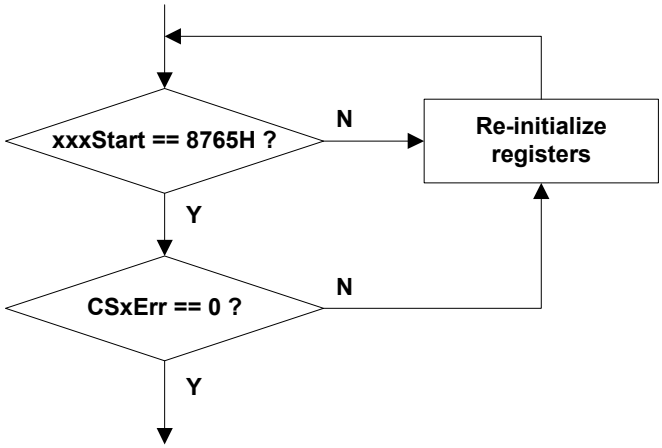



***Figure-6 Check the Effectiveness of Register Value***

### 4.2.2 PL Constant Configuration (PL_Constant)

Energy accumulation and metering are usually referenced by energy unit, such as kWh. However, within the M90E36A, energy calculation or accumulation are based on energy pulse (CF). kWh and CF are connected by Meter Constant (MC, such as 3200 imp/kWh, which means each kWh corresponds to 3200 energy pulses). The chip's PL_Constant is a parameter related to MC. One PL_Constant corresponds to 0.01CF. PL_Constant should be configured according to different MC in application.

The M90E36A provides four energy pulse outputs: active energy pulse CF1, reactive energy pulse or apparent energy pulse CF2, fundamental energy pulse CF3 and harmonic energy pulse CF4. Their Meter Constants are all set by PL_Constant in union rather than separately.

The PL_Constant registers consist of the PLconstH[31H] and PLconstL[32H] registers, corresponding to high word and low word of PL_Constant respectively.

PL_Constant is calculated as below:

PL_Constant = 450,000,000,000 / MC

450,000,000,000: Constant

MC: Meter Constant, unit is imp/KWh, imp/Kvarh or imp/KVA

*Example: Calculation of PL_constant*

Assume:

Meter Constant MC = 3200

Thus:

PL_constant = 450,000,000,000 / 3200

= 140,625,000 (Hex is 8614C68H)

so the registers are set as below:

PLconstH[31H] = 0861H

PLconstL[32H] = 4C68H

### 4.2.3 Metering Method Configuration (MMode0)

The M90E36A can be used in difference systems and metering modes, which can be configured by the MMode0[33H] register.

| Address | Name | Bit15 ~ Bit0 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 33H | MMode0 | Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit9 | Bit8 |
| | | - | - | I1I3Swap | Freq60Hz | HPFOff | didtEn | 001LSB | 3P3W |
| | | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| | | CF2varh | CF2ESV | - | ABSEnQ | ABSEnP | EnPA | EnPB | EnPC |

1 I1I3Swap: this bit defines phase mapping for I1 and I3

0: I1 maps to phase A, I3 maps to phase C (default)

1: I1 maps to phase C, I3 maps to phase A

Note: I2 always maps to phase B.

In PCB layout, the M90E36A may be placed on the top layer or bottom layer. The two placements create input current cross between phase A and C, affecting assembly of the whole meter. The influence can be eliminated by adjusting this control bit.

Note that the swapping of I1and I3 only changes ADC channels and does not affect the chip's internal data processing.

2 Freq60Hz: grid operating line reference frequency

0: 50Hz (default)

1: 60Hz

The M90E36A is applicable in 50 Hz or 60 Hz power grid. The M90E36A uses different calculation parameters in data processing according to different grid frequency. To improve the accuracy of measurement and metering, please set this control bit according to the real power grid frequency.

3 HPFOff: HPF enable control bit

0: enable HPF (default)

1: disable HPF

Besides measuring the voltage/current RMS in 50Hz or 60Hz (AC) power grid, the M90E36A can also measure the mean current value of DC condition. HPF should be disabled when using DC measurement functions.

4 didtEn: enable integrator for didt current sensor

0: disable integrator for didt current sensor; use CT sampling for current channel (default)

1: enable integrator for didt current sensor; use Rogowski coil sampling for current channel

The M90E36A supports sampling over CT or Rogowski coil. Please set this control bit according to the real current sampling means. Note that different sampling circuit should be adopted when using Rogowski coil.

5 001LSB: energy register LSB configuration for all energy registers

0: 0.1CF (default)

1: 0.01CF

6 3P3W: connection type for three-phase energy meter

0: 3P4W connection (default)

1: 3P3W connection

The M90E36A uses different phase sequence judgment for different connection. Please set this control bit according to the real connection type.

7 CF2varh: CF2 pin source configuration

0: apparent energy

1: reactive energy (default)

8 CF2ESV: this bit is to configure the apparent energy computation type when the CF2 pin is set as apparent energy output. This control bit is also used to configure the apparent energy computation type when calculating power factor (PF).

0: All-phase apparent energy arithmetic sum (default)

1: All-phase apparent energy vector sum

9 ABSEnQ: configure the calculation method of total (all-phase-sum) reactive energy and power
0: total reactive energy equals to all-phase reactive energy arithmetic sum (default)
1: total reactive energy equals to all-phase reactive energy absolute sum

10 ABSEnP: configure the calculation method of total (all-phase-sum) active energy and power
0: total active energy equals to all-phase active energy arithmetic sum (default)
1: total active energy equals to all-phase active energy absolute sum

11 EnPA: this bit configures whether Phase A is counted into the all-phase sum energy/power (P/Q/S)
0: Corresponding Phase A not counted into the all-phase sum energy/power (P/Q/S)
1: Corresponding Phase A to be counted into the all-phase sum energy/power (P/Q/S) (default)

12 EnPB: this bit configures whether Phase B is counted into the all-phase sum energy/power (P/Q/S)
0: Corresponding Phase B not counted into the all-phase sum energy/power (P/Q/S)
1: Corresponding Phase B to be counted into the all-phase sum energy/power (P/Q/S) (default)

13 EnPC: this bit configures whether Phase C is counted into the all-phase sum energy/power (P/Q/S)
0: Corresponding Phase C not counted into the all-phase sum energy/power (P/Q/S)
1: Corresponding Phase C to be counted into the all-phase sum energy/power (P/Q/S) (default)

*Application note: Common configuration of MMode0*

(a) 3P4W, grid frequency 50Hz, MMode0 = 0087H

(b) 3P3W, grid frequency 50Hz, MMode0 = 0185H

### 4.2.4 PGA Gain Configuration (MMode1)

The MMode1 register is used to configure PGA gain of ADC sampling channel, making chips applicable to meter designs of different current specifications.

| Address | Name | Bit15 ~ Bit0 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 34H | MMode1 | Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit9 | Bit8 |
| | | DPGA_GAIN | | PGA_GAIN (V3) | | PGA_GAIN (V2) | | PGA_GAIN (V1) | |
| | | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| | | PGA_GAIN (I4) | | PGA_GAIN (I3) | | PGA_GAIN (I2) | | PGA_GAIN (I1) | |

1 DPGA_GAIN: digital PGA gain for the 4 current channels
00: Gain = 1 (default)
01: Gain = 2
10: Gain = 4
11: Gain = 8

2 PGA_GAIN (V1~V3, I1~I4): analog PGA gain for seven ADC channels
00: 1X (default)
01: 2X
10: 4X
11: N/A

*Application note: Configuration principle of PGA gain*

(a) Ensure that the ADC channel analog input signal should be within the dynamic range of 0~720mVrms

(b) Configure PGA gain to be the maximum value within the whole dynamic range

### 4.2.5 Offset Calibration of Voltage/ Current/ Power

In application, the input signal is often influenced by the interference signal. This interference will enter data processing module through ADC and high-pass filter, not only producing errors to the voltage/current RMS and power calculation, but also affecting accuracy of the energy metering. The M90E36A provides offset calibration function to voltage, current and power, reducing the influence of the interference signal to measurement/metering accuracy.

Every phase's voltage/current offset calibration should be proceeded individually. Take phase A for example, the signal source is: Ub=Uc=Un, Ua=0, Ia=0. The calibration flow of voltage/current offset is as below:

*a.* Read measurement registers (32 bits). It is suggested to read several times to get the average value;
*b.* Right shift the 32-bit data by 7 bits (ignore the lowest 7 bits);
*c.* Invert all bits and add 1 (2's complement);
*d.* Write the lower 16-bit result to the offset register

Every phase's power offset calibration should be proceeded individually. Take phase A for example, the signal source is: Ua=Ub=Uc=Un, Ia=0. Set the input source to be 0, the calibration flow of power offset is as below:

*a.* Read measurement registers (32 bits). It is suggested to read several times to get the average value;
*b.* Calculate: register value x 100,000 / 65,536
*c.* Right shift the caculated result data by 8 bits (ignore the lowest 8 bits);
*d.* Invert all bits and add 1 (2's complement);
*e.* Write the lower 16-bits result to the offset register

The relationship between offset register and measurement register is as below:

| Item | Data Width | Data Align | | | Minimum Unit |
|---|---|---|---|---|---|
| voltage rms | 32 bits | 9 bits | 16 bits | 7 bits | 0.02mV |
| current rms | 32 bits | 9 bits | 16 bits | 7 bits | 0.2μA |
| mean power | 32 bits | 8 bits | 16 bits | 8 bits | 0.00256W |
| | | | Offset register | | |

The corresponding offset register and measurement value registers are shown as below:

| | Offset Registers | | Measurement Value Registers | | | |
|---|---|---|---|---|---|---|
| | Address | Register Name | Address | Register Name | Address | Register Name |
| Voltage | 63H | UoffsetA | 0D9H | UrmsA | 0E9H | UrmsALSB |
| | 67H | UoffsetB | 0DAH | UrmsB | 0EAH | UrmsBLSB |
| | 6BH | UoffsetC | 0DBH | UrmsC | 0EBH | UrmsCLSB |
| Current | 64H | IoffsetA | 0DDH | IrmsA | 0EDH | IrmsALSB |
| | 68H | IoffsetB | 0DEH | IrmsB | 0EEH | IrmsBLSB |
| | 6CH | IoffsetC | 0DFH | IrmsC | 0EFH | IrmsCLSB |
| | 6EH | IoffsetN | 0D8H | IrmsN1 | - | - |
| All-wave Power | 41H | PoffsetA | 0B1H | PmeanA | 0C1H | PmeanALSB |
| | 42H | QoffsetA | 0B5H | QmeanA | 0C5H | QmeanALSB |
| | 43H | PoffsetB | 0B2H | PmeanB | 0C2H | PmeanBLSB |
| | 44H | QoffsetB | 0B6H | QmeanB | 0C6H | QmeanBLSB |
| | 45H | PoffsetC | 0B3H | PmeanC | 0C3H | PmeanCLSB |
| | 46H | QoffsetC | 0B7H | QmeanC | 0C7H | QmeanCLSB |
| fundamental power | 51H | PoffsetAF | 0D1H | PmeanAF | 0E1H | PmeanAFLSB |
| | 52H | PoffsetBF | 0D2H | PmeanBF | 0E2H | PmeanBFLSB |
| | 53H | PoffsetCF | 0D3H | PmeanCF | 0E3H | PmeanCFLSB |

### 4.2.6 Voltage/ Current Measurement Calibration

Measurement calibration means the calibration of voltage rms (Urms) gain and current rms (Irms) gain. Measurement calibration is the premise of energy metering calibration.

1 Voltage/current offset (Uoffset/Ioffset) calibration:
For calibration method, please refer to 4.2.5 Offset Calibration of Voltage/ Current/ Power. No need of calibration if the voltage/current offset is very small in general application.

2 Voltage/current gain calibration:
The three phases' calibration can be proceeded simultaneously. The signal source is: Ua=Ub=Uc=Un, Ia=Ib=Ic=In(Ib). The calibration method is as below:

*a.* Read *voltage*/current value of the external reference meter, and also read the voltage/current measurement value from chip registers;

*b.* Calculate the voltage/current gain:

$$\text{Voltage Gain} = \frac{\text{reference voltage value}}{\text{voltage measurement value}} \times 52800$$

$$\text{Current Gain} = \frac{\text{reference current value}}{\text{current measurement value}} \times 30000$$

*c.* Write the result to the corresponding voltage/current gain registers

Note: voltage/current gain calibration is not necessarily proceeded when gain register is the default value. That is, when the first calibration result is not ideal, there is no need to reset the gain register to the default value. Calibration can be performed again based on the current value. The formula is as below:

$$\text{New Voltage Gain} = \frac{\text{reference voltage value}}{\text{voltage measurement value}} \times \text{existing voltage gain}$$

$$\text{New Current Gain} = \frac{\text{reference current value}}{\text{current measurement value}} \times \text{existing current gain}$$

The corresponding voltage/current gain register and measurement value registers are shown as below:

| | Gain Register | | Measurement Value Registers | | | |
|---|---|---|---|---|---|---|
| | **Address** | **Register Name** | **Address** | **Register Name** | **Address** | **Register Name** |
| Voltage | 61H | UgainA | 0D9H | UrmsA | 0E9H | UrmsALSB |
| | 65H | UgainB | 0DAH | UrmsB | 0EAH | UrmsBLSB |
| | 69H | UgainC | 0DBH | UrmsC | 0EBH | UrmsCLSB |
| Current | 62H | IgainA | 0DDH | IrmsA | 0EDH | IrmsALSB |
| | 66H | IgainB | 0DEH | IrmsB | 0EEH | IrmsBLSB |
| | 6AH | IgainC | 0DFH | IrmsC | 0EFH | IrmsCLSB |
| | 6DH | IgainN | 0D8H | IrmsN1 | - | - |

**Application Note:**

(a) Voltage rms is unsigned and the minimum unit 1LSB of the UrmsA/UrmsB/UrmsC registers is 0.01V. Only the higher 8 bits of the UrmsALSB/UrmsBLSB/UrmsCLSB registers are valid, the lower 8 bits are always 0, and 1LSB is 0.01/256 V.

(b) Current rms is unsigned and the minimum unit 1LSB of the IrmsA/IrmsB/IrmsC registers is 0.001A; Only the higher 8 bits of the IrmsALSB/IrmsBLSB/IrmsCLSB registers are valid, the lower 8 bits are always 0, and 1LSB is 0.001/256 A.

*Example: Voltage gain calibration*

Assume:

The initial value of phase A voltage gain register UgainA is 0CE40H (52800)

Reference meter output voltage is 220.00V

Voltage rms register readout UrmsA = 5BA0H (23456)

The higher 8 bits of voltage LSB register readout UrmsALSB = 4EH (78)

Thus:

voltage measured value = (UrmsA x 0.01) + (UrmsALSB x 0.01 / 256)

= (23456 x 0.01) + (78 x 0.01 / 256)

=234.563 V

voltage gain = 220.00 / 234.563 x 52800 = 49521.88 = 0C172H

So the register can be set to:

UgainA = 0C172H

### 4.2.7 Energy Metering Calibration

Only active energy is required for energy calibration. There is no need to calibrate reactive energy, the accuracy of which is guaranteed by chip design. Metering calibration flow is gain first then phase angle. Active energy pulse output (CF1) should be connected to the pulse input port of the calibration bench during calibration.

Energy metering should be calibrated at In (Ib).

1 Power offset (Poffset/Qoffset) calibration
For calibration method please refer to 4.2.5 Offset Calibration of Voltage/ Current/ Power. No need of calibration if the power offset is very small in general application.

2 Gain calibration
Every phase's gain calibration should be proceeded individually. Take phase A for example, the signal source is: Ua=Ub=Uc=Un, Ia=In(Ib), Ib=Ic=0, PF=1.0. The calibration method is as below:
*a.* Read the energy error value e from calibration bench;
*b.* Calculate the gain;

$$Gain = \text{Complementary}\left(\frac{-\varepsilon}{1+\varepsilon} \text{ x } 2^{15}\right)$$

*c.* Write the result to the corresponding gain registers.

3 Phase angle calibration. Take phase A for example, the signal source is: Ua=Ub=Uc=Un, Ia=In(Ib), Ib=Ic=0, PF=0.5L.The calibration method is as below:
*a.* Read the energy error value $e_p$ from calibration bench;
*b.* Calculate the phase angle error;

$$AngleError = \varepsilon_p * \text{Gphase}$$

Gphase is a constant. When grid frequency is 50Hz, Gphase=3763.739. When grid frequency is 60Hz, Gphase=3136.449
*c.* Write the result to the corresponding phase angle error registers. The phase angle registers are signed and MSB of 1 indicates a negative value.

The corresponding gain register and phase angle registers are shown as below:

| | Address | Register Name |
|---|---|---|
| **Phase A** | 47H | GainA |
| | 48H | PhiA |
| **Phase B** | 49H | GainB |
| | 4AH | PhiB |
| **Phase C** | 4BH | GainC |
| | 4CH | PhiC |

*Example: Energy gain and phase angle calculation*

The condition is that power factor PF=1.0, current is $I_b$, energy error ε is -13.78%, so:

-ε/(1+ε)=0.159823707,

gain = int(0.159823707* 2^15)=5237.10=1475H

Write 1475H to the gain register.

After gain calibration, energy error $\varepsilon_P$ is 0.95% in the condition of PF=0.5L, current is $I_b$ and frequency is 50Hz, so:

phase angle = $\varepsilon_P$*3763.739

=0.0095*3763.739=35.75553=24H;

Write 24H to the phase angle register.

### 4.2.8 Fundamental Energy Metering Calibration

For fundamental energy metering calibration, only gain and offset calibration is needed. There is no need to calibrate phase angle. Fundamental energy pulse output (CF3) should be connected to the pulse input port of the calibration bench during calibration.

The startup register for fundamental energy metering calibration is HarmStart [50H]. Calibration related registers are 51H~56H. During calibration, please only start and configure these registers rather than other registers.

Fundamental energy metering calibration is similar to energy metering calibration.

1 Fundamental power offset (PoffsetxF) calibration

For fundamental power offset calibration, only active power error needs to be calibrated per phase individually. Take phase A for example, the signal source is: Ua=Ub-Uc=Un, Ia=0. For calibration method please refer to 4.2.5 Offset Calibration of Voltage/ Current/ Power. No need of calibration if the power offset is very small in general application.

2 Fundamental energy gain calibration

Every phase's fundamental energy calibration should be proceeded individually. Take phase A for example, the signal source is: Ua=Ub=Uc=Un, Ia=In(Ib), Ib=Ic=0, PF=1.0. The calibration method is as below:

*a.* Read the error value e from the external reference meter;

*b.* Calculate the gain;

$$Gain = \text{Complementary}\left(\frac{-\varepsilon}{1+\varepsilon} \text{ x } 2^{15}\right)$$

*c.* Write the result to the corresponding gain registers.

The corresponding fundamental energy gain registers are shown as below:

| Address | Register Name |
|---|---|
| 54H | PGainAF |
| 55H | PGainBF |
| 56H | PGainCF |

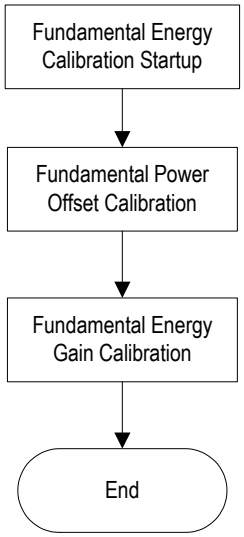



***Figure-7 Fundamental Energy Metering Calibration Flow***

## 4.3 CALIBRATION IN PARTIAL MEASUREMENT MODE

Partial measurement related registers are 14H~1DH. There are no specific startup and checksum registers. Therefore, the related register should be cleared and configured with initial values before calibration.

### 4.3.1 Partial Measurement Configuration (PMConfig)

| Address | Register Name | Bit15 ~ Bit0 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 1BH | PMConfig | Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit9 | Bit8 |
| | | - | ReMeasure | MeasureStartZX | MeasureType | - | - | - | - |
| | | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| | | - | - | - | - | - | - | - | PMBusy |

1 ReMeasure: enable another measurement cycle
  0: not enable (default)
  1: trigger another measurement cycle
  The partial measurement module is one-time triggered, that is, once the ReMeasure bit is set, current measurement is performed one time then turned off. If measurement is required again, the ReMeasure bit should be set again.
2 MeasureStartZX: configure start of measurement
  0: Measurement start immediately after the ReMeasure bit is set (default)
  1: Measurement start from zero-crossing point after the ReMeasure bit is set
3 MeasureType: indicate the measurement type
  0: RMS measurement (default)
  1: Mean Value (DC Average) measurement
4 PMBusy: indicate the measure ‘Busy’ status
  0: Measurement done (default)
  1: Measurement in progress, ‘Busy’

### 4.3.2 Sampling Cycle Configuration (PMAvgSamples)

The PMAvgSamples[1CH] register is used to configure the partial measurement sampling cycle. The unit is the number of ADC sampling within a partial measurement cycle. The default grid frequency is 50Hz, so at the ADC sampling rate of 8K, the default value of PMAvgSamples is 160 (0A0H).

### 4.3.3 PGAgain Configuration (PMPGA)

The ADC PGAgain Configuration in Partial Measurement mode is similar to the MMode1 configuration in Normal mode.

| Address | Register Name | Bit15 ~ Bit0 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 17H | PMPGA | Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit9 | Bit8 |
| | | DPGA_GAIN | | - | - | - | - | - | - |
| | | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| | | - | - | PGA_GAIN (I3) | | PGA_GAIN (I2) | | PGA_GAIN (I1) | |

1 DPGA_GAIN: DPGA gain for four current sampling channels
  00: Gain = 1 (default)
  01: Gain = 2
  10: Gain = 4
  11: Gain = 8
2 PGA_GAIN(I1~I3): PGA gain for three ADC sampling channels
  00: Gain = 1 (default)
  01: Gain = 2
  10: Gain = 4
  11: N/A

### 4.3.4 Current Offset Calibration

Considering the influence of the interference signal, Partial Measurement mode also supports current offset calibration. The calibration method is slightly different from the current offset calibration in Normal mode. Take the rms measurement for example, the calibration method is as below:

*a.* Set the input source to be 0;
*b.* Set MeasureType=1 and ReMeasure=1 to start one current measurement;
*c.* Read the current registers (16 bits) after measurement completion
*d.* Repeat step b and c. It is suggested to read many times to get the average value;
*e.* Invert all bits and add 1 (2's complement);
*f.* Write the result to the corresponding offset register

| Offset Registers | | Measurement Value Registers | |
|---|---|---|---|
| **Address** | **Register Name** | **Address** | **Register Name** |
| 14H | PMoffsetA | 18H | PMIrmsA |
| 15H | PMoffsetB | 19H | PMIrmsB |
| 16H | PMoffsetC | 1AH | PMIrmsC |

Partial Measurement module also provides the measurement value LSB register PMIrmsLSB. This register value has different definition in rms measurement (AC) and Mean Value measurement (DC) as shown below:

| Address | Register Name | Bit15 ~ Bit0 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 1DH | PMIrmsLSB | Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit9 | Bit8 |
| | | - | - | - | - | IrmsCLSB | | | |
| | | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| | | IrmsBLSB | | | | IrmsALSB | | | |

In rms measurement, the PMIrmsLSB register value is the LSB of the measurement value. In mean value measurement, this register value is the MSB of the measurement value.

#### 4.3.5 Current Measurement Calibration

The M90E36A only has current measurement function in Partial Measurement mode, so current gain needs to be calibrated. Current gain calibration for three phases can be proceeded simultaneously. Take rms measurement for example, the calibration method is as below:

*a.* Set MeasureType=0 and ReMeasure=1 to start one current measurement;
*b.* Read the current value from the signal source (reference meter) and read the value of current registers (16 bits);
*c.* Calculate the current gain
Current gain = reference current value / current measurement value
*d.* Partial Measurement mode has no special current gain register, so the calculated result should be saved in MCU or external memory.

Note that the partial measurement module is enabled in both Normal and Partial Measurement mode. That means the partial measurement module can measure current value in both modes.

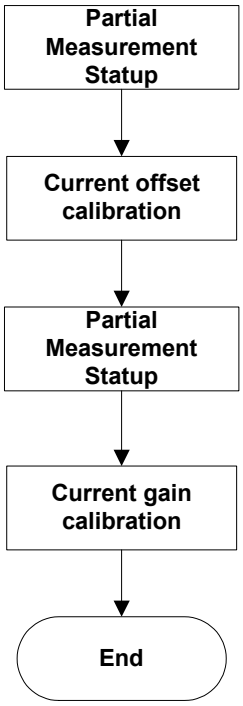



***Figure-8 Partial Measurement Calibration Flow***

#### 4.3.6 Special Application of Partial Measurement Function

In Normal mode, the current rms measurement uses 16 cycles as the measurement period, that means current measurement period is 320ms when grid frequency is 50Hz. If there is a need to measure current at special period, start partial measurement function in Normal mode, and proceed specific period current measurement by configuring the partial measurement sampling period register PMAvgSamples. It is noted that employing specific period current measurement function will not influence the energy metering and parameters measurement functions in Normal mode, since the partial measurement module is also active in Normal mode.

The partial measurement module can proceed RMS measurement (AC) and Mean Value measurement (DC). The mean value measurement can also be proceeded in Normal mode by starting partial measurement function.

*Application note: How to measure DC current signal*

DC measurement function is proceeded by partial measurement module. The flow of DC measurement is as below:

*a.* Disable HPF (HPFOff=1)
*b.* Set MeasureType to 1
*c.* Set ReMeasure to start current measurement once
*d.* Detect the IRQ0 pin or the PMBusy bit to judge whether measurement is completed
*e.* Read the PMIrmsA/PMIrmsB/PMIrmsC/PMIrmsLSB registers to get measurement result
*f.* Repeat step c~e if to measure again

## 4.4 CALIBRATION IN DETECTION MODE

Current detection is realized by low power consumption comparators. The comparator outputs low level when the external current is lower than the configured threshold; The comparator outputs high level when the external current is higher than the configured threshold, as shown in Figure-9.

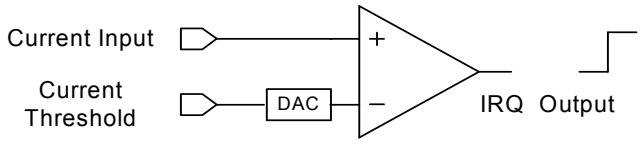



***Figure-9 Current Detection Principle***

### 4.4.1 Current Detection Module Configuration

Six current threshold comparators can be configured for the current detection module to detect positive and negative current of three phases. These six threshold comparators can be enabled and disabled by the control bits, as shown below:

| Address | Register Name | Bit15 ~ Bit0 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 10H | DetectCtrl | Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit9 | Bit8 |
| | | - | - | - | - | - | - | - | - |
| | | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| | | - | - | PDN3 | PDN2 | PDN1 | PDP3 | PDP2 | PDP1 |

1 PDN3/2/1: Control bits for negative detector of channel 3/2/1;
  0: Detector enable (default)
  1: Detector disable
2 PDP3/2/1: Control bits for positive detector of channel 3/2/1;
  0: Detector enable (default)
  1: Detector disable

Each of the six current threshold comparators has its own register configuration as shown below:

| Address | Register Name | Bit15 ~ Bit0 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 11H<br>12H<br>13H | DetectThA<br>DetectThB<br>DetectThC | Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit9 | Bit8 |
| | | - | CalCodeN | | | | | | |
| | | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| | | - | CalCodeP | | | | | | |

1 CalCodeN: negative detector threshold, 7-bit width.
  7'b000-0000 corresponds to minimum threshold Vc=-4.28mV=-3.03mVrms
  7'b111-1111 corresponds to maximum threshold Vc=12.91mV=9.14mVrms
2 CalcodeP: positive detector threshold, definition is the same as CalCodeN.

### 4.4.2 Current Detection Threshold Calibration

Because of the low power consumption consideration and the manufacturing process, the current detection threshold is different from different chips. Therefore, calibration is needed due to the offset of chip's DAC output (less than ±5mVrms). The threshold current range is 2mVrms ~ 4mVrms within which the current detection module (low power consumption comparator) can detect accurately. It is recommended to proceed system design according to current detection threshold of 3mVrms.

In Detection mode, all registers are not accessible, so the current threshold registers need to be configured in Normal mode first before entering Detection mode.

Dichotomy is suggested in current detection threshold calibration. The recommended calibration flow is as shown in Figure-10.

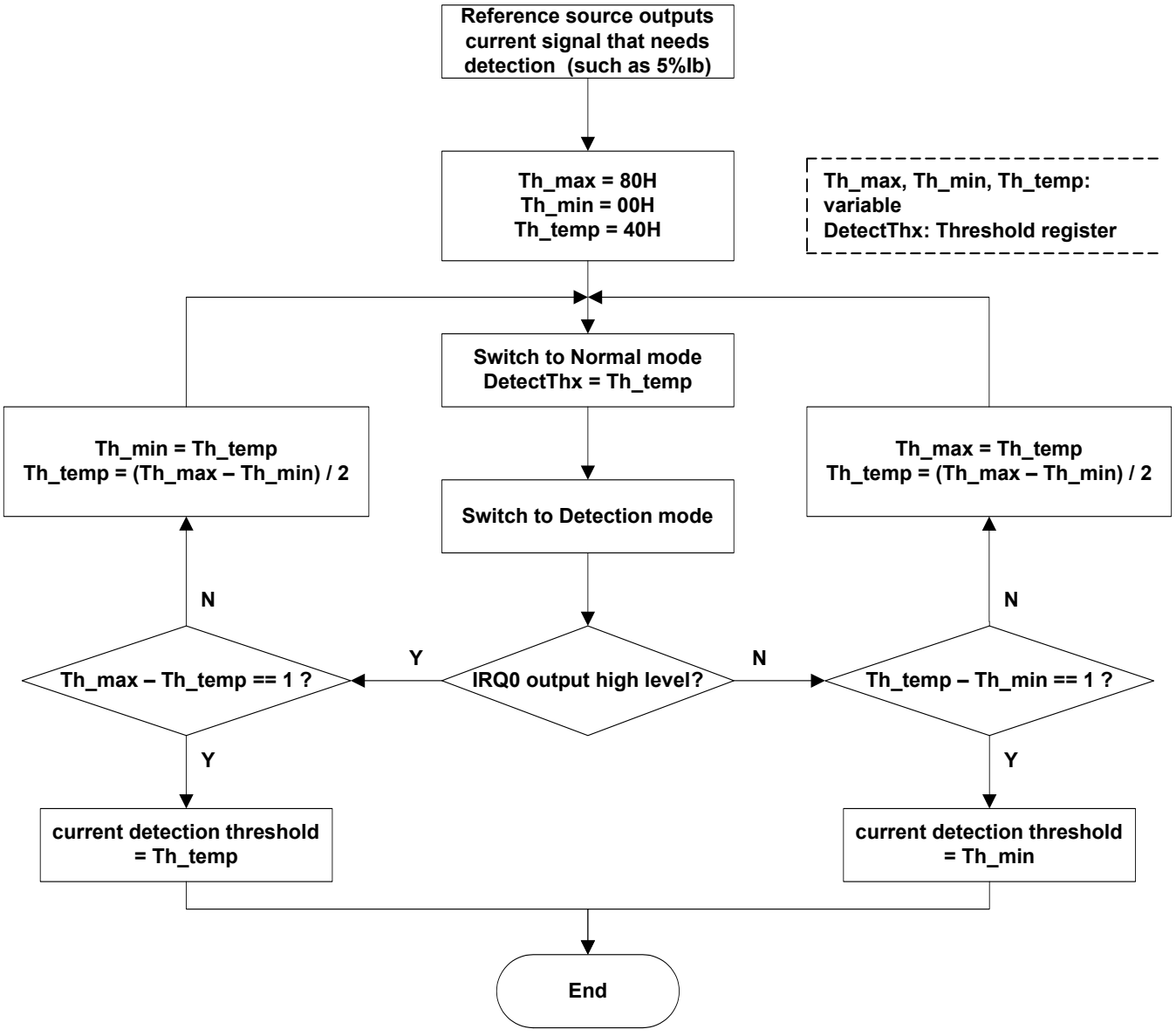



*Figure-10 Current Detection Threshold Calibration Flow*

# 5 FUNCTION REGISTERS CONFIGURATION

## 5.1 STARTUP CURRENT CONFIGURATION

The registers which related to startup current configuration is shown as below:

| Address | Register Name | Description |
|---|---|---|
| 35H | PStartTh | All-phase Active Startup Power Threshold. |
| 36H | QStartTh | All-phase Reactive Startup Power Threshold. |
| 37H | SStartTh | All-phase Apparent Startup Power Threshold. |
| 38H | PPhaseTh | Each-phase Active Startup Power Threshold. |
| 39H | QPhaseTh | Each-phase Reactive Startup Power Threshold. |
| 3AH | SPhaseTh | Each-phase Apparent Startup Power Threshold. |

1 Due to system interference when current is 0, small signal may be gernerated in current sampling channel, producing a certain amount of energy and affecting the measurement and metering accuracy. To avoid this, the M90E36A provides the each-phase startup power configuration/judgment function.

2 PPhaseTh, QPhaseTh and SPhaseTh are used to judge the startup power of each phase (A/B/C). Take active power for example, when a single phase input power is smaller than the configured PPhaseTh value, the input active power of that phase will be set to 0 by force, that means input to the next process is 0. Otherwise the signal will be streamed to the next process.
Note that the threshold are configured separately to active(P), reactive(Q) and apparent (S). The compared value is (|P|+|Q|).

3 PStartTh, QStartTh and SStartTh are used to judge all-phase startup power. Take active power for example, when all-phase-sum power is less than the configured PStartTh value, energy accumulation will not start. Otherwise energy accumulation will start.

4 Calculation methods of the two register groups are the same. The formula is as below:
Register value = N / 0.00032, (N is the configured power threshold).

*Example: Startup Current Configuration*

Assume:

meter voltage is 220V, current specification 5(100)A, active startup current is 0.1%

Considering the accuracy of current measurement in small-current state, it is recommended to configure the all-phase startup current threshold to be 50% of startup current (also can configure based the actual conditions).

Assume the startup threshold of each-phase power is configured to be 10% of startup current.

so:

All-phase Active Startup Power Threshold = 3 x 5 x 0.1% x 50% x 220 = 1.65W

Each-phase Active Startup Power Threshold = 5 x 0.1% x 10% x 220 = 0.11W

Register values are:

PStartTh[35H] = 1.65 / 0.00032 = 5156 = 1424H

PPhaseTh[38H] = 0.11 / 0.00032 = 344 = 158H

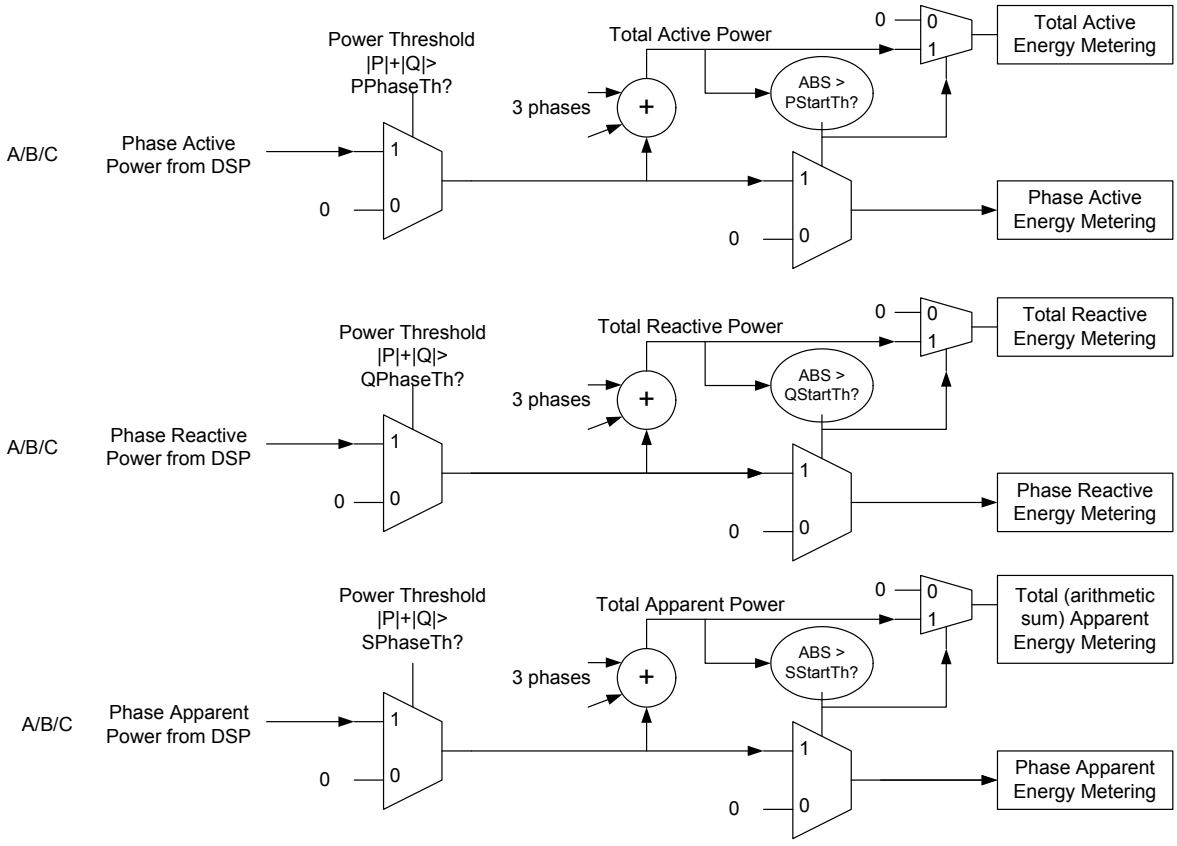



***Figure-11 Metering Startup Handling***

## 5.2 SAG FUNCTION

Sag detect function is provided in M90E36A. The threshold of sag detection is configured through the SagTh register (08H). All three voltage phases use the same threshold. The threshold equation is as below:

$$SagTh = \frac{Vth \times 100 \times \sqrt{2}}{2 \times Ugain / 32768}$$

Vth: the voltage threshold to be configured;

Ugain: the gain after calibration

The default value of the SagTh register (08H) is 0000H. It is suggested to set the SagTh register (08H) appropriately even if the Sag function is not used in application. The reasons are as follows:

In normal mode, all measurement values are calculated based on the average cycle out of 16 voltage cycles. And the voltage cycle makes use of the internal zero-crossing signal, which is different from the output on the ZX2 / ZX1 / ZX0 pins.

In a 3P4W system, this internal zero-crossing signal is based on phase A voltage $U_a$ firstly. If phase A is in sag, phase C voltage Uc is switched. If phase A and phase C are both in sag, phase B voltage Ub is switched. In a 3P3W system, the internal zero-crossing signal is based on phase A voltage Uab firstly. If phase A is in sag, phase C voltage Ucb is switched. In either 3P4W and 3P3W application, if all phases are in sag, the average cycle of 16 voltage cycles is calculated in accordance with the configured reference frequency (50 Hz or 60 Hz), i.e. 320ms for 50Hz system and 266.7ms for 60Hz system.

However, for energy meter or power instrument with auxiliary power supply, if the SagTh register is not configured (the default power-on value is 0), the M90E36A will not enter sag even if there is no signal on voltage circuits due to the interference noise. Thus the wrong average cycle might be used to calculate measurement values such as current rms.

## 5.3 RESERVED REGISTER/ ADDRESS AND RESERVED BITS

### 5.3.1 Reserved Register/ Address

The M90E36A has many reserved registers and non-listed address areas besides the registers listed in datasheet. These reserved registers are not open to users. Please don't operate on the address outside of the datasheet. Access to reserved register/address needs special operation because normal operation can not make change or impact to these register values.

### 5.3.2 Reserved Register Bits

Some fields of defined registers in the datasheet are labeled as 'reserved'. In application, all the reserved bit fields shall be written with '0' when those bits have to be written, and shall be masked out (hence ignored) upon read.

### 5.3.3 Reserved Bits in the FUNC_EN1 Register

The most registers' reserved bits will return 'fixed 0' upon read. There is only one exception: the FUNC_EN1 register (04H). This register has three reserved bits. Those bits may return non-fixed value upon read. Users need to mask out or ignore those bits when using the read-back value of this register. Please note that the non-fixed return value does not indicate any abnormal working condition of the internal hardware logic. Users just need to ignore those bit fields.

| Address | Name | Bit15 ~ Bit0 | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| 04H | FuncEn1 | Bit15 | Bit14 | Bit13 | Bit12 | Bit11 | Bit10 | Bit9 | Bit8 |
| | | INOv1En | INOv0En | Reserved | Reserved | THDUOvEn | THDIOvEn | DFTDone | Reserved |
| | | Bit7 | Bit6 | Bit5 | Bit4 | Bit3 | Bit2 | Bit1 | Bit0 |
| | | RevQchg-TEn | RevQch-gAEn | RevQchg-BEn | RevQchg-CEn | RevPchg-TEn | RevPch-gAEn | RevPchg-BEn | RevPchg-CEn |

# 6 TEMPERATURE COMPENSATION

The M90E36A itself embodies good temperature characteristic. Considering that the external components might be affected by temperature in application, the M90E36A also provides compensation function for external temperature drift.

A series of special registers should be configured for temperature compensation. These registers are located in special addresses, and access to these registers should be strictly carried out as the following.

## 6.1 ON-CHIP TEMPERATURE SENSOR CONFIGURATION

The M90E36A provides a built-in temperature sensor. Due to the manufacturing process, the temperature sensor might be somewhat different for different chips. Therefore the on-chip temperature sensor should be configured before temperature compensation.

The configuration method is as below:

*a.* Write AA55H to address 2FDH
*b.* Write 5122H to address 216H
*c.* Write 012BH to address 219H
*d.* Write 0000H to address 2FDH

Read the Temp[0FCH] register directly to get the current temperature after configuration completed. Please note that, the temperature sensor will sense the temperature of the chip and it may have a few degrees of difference between the chip junction temperature and ambient temperature.

## 6.2 TEMPERATURE COMPENSATION BASED ON ADC SAMPLING CHANNEL

The temperature compensation method is as below:

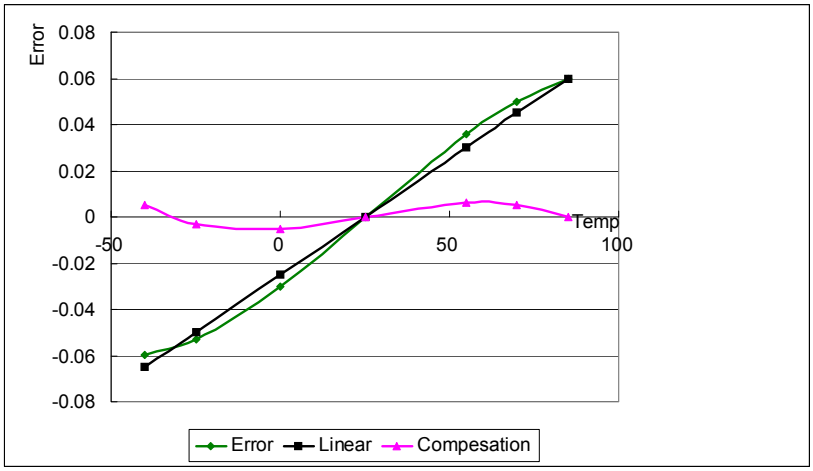
*a.* Write AA55H to address 2FCH
*b.* Write the temperature coefficient to be compensated to address 270H
*c.* Write the fiducial point temperature of the temperature coefficient to address 27BH
*d.* Write 0000H to address 2FCH

The reference point temperature of the temperature coefficient is generally configured to be the temperature in calibration. That is, in calibration, read the Temp[0FCH] register first to get the current temperature and then save it as the reference temperature.

| Address | Register Name | Bit | Read/Write | Default Value | Description |
|---|---|---|---|---|---|
| 270H | TempCompGain | 15:8 | Read/Write | 0 | Reserved bit. Readout value is 0. |
| | | 7:0 | - | - | Temperature compensation coefficient, bit 7 is the sign bit, unit is ppm/ ℃ |
| 27BH | TempCompRef | 15 | Read/Write | 0 | 1: enable temperature compensation<br>0: disable temperature compensation |
| | | 14:9 | - | - | Reserved bit. Readout value is 0 |
| | | 8:0 | Read/Write | 19H | The reference temperature of the temperature coefficient, bit 8 is the sign bit, unit is ℃ |

*Example:*

Test data before temperature compensation is as below:




After linearization:

The reference temperature (temperature in calibrating) is 25 ℃ , metering error is 0.0000%;

The error at 85 ℃ point is 0.06%

So the temperature coefficient is calculated as below:

(0.06% - 0.0000%) / (85 ℃ - 25 ℃ ) = 10ppm/ ℃

The temperature coefficient to be compensated is -10ppm/ ℃ . Register configuration is as below:

*a.* Write AA55H to address 2FCH
*b.* Write FFF6H to address 270H
*c.* Write 8019H to address 27BH
*d.* Write 0000H to address 2FCH

## 6.3 TEMPERATURE COMPENSATION BASED ON REFERENCE VOLTAGE

On-chip high-precision reference voltage is provided with excellent low temperature coefficient. But in application, what should be considered is the temperature drift of the whole system. Therefore, the M90E36A specially provides temperature compensation based on reference voltage to minimize temperature drift caused by the on-board components.

Note that, as voltage and current ADC sampling adopt the same reference voltage, compensation on the reference voltage will bring double effect on power and energy.

Temperature compensation on reference voltage is proceeded with every 8 ℃ as a segment. In application, it is suggested to test on a small batch of components from the same lot to get the best temperature compensation coefficient. And then use this compensation coefficient as a fixed value to be written directly to register in production.

The temperature compensation method is as below:

*a.* Write AA55H to address 2FDH
*b.* Write the reference voltage coefficient of segmented compensation to addresses 202H~209H
*c.* Write the curvature of segmented compensation curve to address 201H
*d.* Write 0000H to address 2FDH

In normal condition, reference voltage is 1200mV. The unit of reference voltage compensation is 0.020mV in this compensation method.

The default value of the corresponding compensation registers is the ideal value in chip design. In application, only incremental adjustment is needed.

| Address | Register Name | Bit | Read/Write | Default Value | Description |
|---|---|---|---|---|---|
| 201H | BGCurveK | 15:4 | - | - | Reserved bit, readout value is 0 |
| | | 3:0 | Read/Write | 0 | Reference voltage temperature compensation curve.<br>The bit3 is assumed as sign bit, range is -8 to +7.<br>Scaling factor = 1+ register value*1/8.<br>So the scaling factor will be from 0, with step of 1/8, all the way to 1+7/8. |
| 202H | BG_TEMP_P12 | 15:8 | Read/Write | 0 | Compensation coefficient on the 25 ℃ temperature point |
| | | 7:0 | Read/Write | 1 | Compensation coefficient on the 17 ℃ temperature point |
| 203H | BG_TEMP_P34 | 15:8 | Read/Write | 6 | Compensation coefficient on the 41 ℃ temperature point |
| | | 7:0 | Read/Write | 2 | Compensation coefficient on the 33 ℃ temperature point |
| 204H | BG_TEMP_P56 | 15:8 | Read/Write | 25 | Compensation coefficient on the 57 ℃ temperature point |
| | | 7:0 | Read/Write | 13 | Compensation coefficient on the 49 ℃ temperature point |
| 205H | BG_TEMP_P78 | 15:8 | Read/Write | 53 | Compensation coefficient on the 73 ℃ temperature point |
| | | 7:0 | Read/Write | 39 | Compensation coefficient on the 65 ℃ temperature point |
| 206H | BG_TEMP_N12 | 15:8 | Read/Write | 16 | Compensation coefficient on the 1 ℃ temperature point |
| | | 7:0 | Read/Write | 6 | Compensation coefficient on the 9 ℃ temperature point |
| 207H | BG_TEMP_N34 | 15:8 | Read/Write | 54 | Compensation coefficient on the -15 ℃ temperature point |
| | | 7:0 | Read/Write | 34 | Compensation coefficient on the -7 ℃ temperature point |
| 208H | BG_TEMP_N56 | 15:8 | Read/Write | 117 | Compensation coefficient on the -31 ℃ temperature point |
| | | 7:0 | Read/Write | 79 | Compensation coefficient on the -23 ℃ temperature point |
| 209H | BG_TEMP_N78 | 15:8 | Read/Write | 205 | Compensation coefficient on the -47 ℃ temperature point |
| | | 7:0 | Read/Write | 159 | Compensation coefficient on the -39 ℃ temperature point |

# 7 HARMONIC ANALYSIS

## 7.1 DFT ENGINE

The built-in DFT computation engine supports 2nd-32nd order harmonic analysis function for 6 channels. The calculation error will be enlarged when input signal is small. To address this issue, a prescaler is designed and placed before the DFT engine to amplify the signal to be calculated.

The designed ADC sampling rate is 8kHz. Harmonic analysis adopts 4096 sampling points for DFT computation which takes around 0.5s once.

Considering there are many DFT computation outputs, the DFT computation engine is closed by default to ensure external MCU can read DFT data from the same calculation. The engine needs to be enabled to startup, and it will automatically shut off after completing calculation for one time. Calculation results are stored in registers. External MCU can read these registers to get calculation results through SPI interface.

Harmonic measurement accuracy is guaranteed by chip design after voltage/current calibration.

The control registers of DFT computation engine is as below:

| Address | Register Name | Bit | Read/Write | Default Value | Description |
|---|---|---|---|---|---|
| 1D0H | DFT_SCALE | 15 | Read/Write | 0 | 0: Enable Hanning window<br>1: Disable Hanning window |
| | | 14:13 | Read/Write | 0 | Voltage scale for phase C. |
| | | 12:11 | Read/Write | 0 | Voltage scale for phase B. |
| | | 10:9 | Read/Write | 0 | Voltage scale for phase A. |
| | | 8:6 | Read/Write | 0 | Current scale for phase C. |
| | | 5:3 | Read/Write | 0 | Current scale for phase B. |
| | | 2:0 | Read/Write | 0 | Current scale for phase A. |
| 1D1H | DFT_CTRL | 15:1 | - | 0 | Reserved bit. |
| | | 0 | Read/Write | 0 | 0: Disable DFT engine<br>1: Enable DFT engine |

1 The function of Hanning window is to bring periodicity to ADC sampling signal in DFT computation to achieve the exact calculation result. Please enable Hanning window in general application.

2 Voltage scale, InputGain= 2^Scale
- 00: Gain = 1
- 01: Gain = 2
- 10: Gain = 4
- 11: Gain = 8

3 Current scale, InputGain= 2^Scale
- 000: Gain = 1
- 001: Gain = 2
- 010: Gain = 4
- 011: Gain = 8
- 100: Gain = 16
- 101: Gain = 32
- 110: Gain = 64
- 111: Gain = 128

4 DFT engine switch: DFT computation engine is enabled after setting the DFT_CTRL bit. This bit will be cleared automatically after completing calibration for one time. In application, this bit can be used to judge whether DFT computation is completed.

DFT application is as below:

*a.* Set DFT computation engine and write 2A49H to the DFT_SCALE [1D0H] register (Assume gain of voltage and current is two)
*b.* Start DFT computation engine and write 001H to the DFT_CTRL [1D1H] register
*c.* Check DFT_CTRL. If DFT_CTRL=0, DFT computation is completed (about 0.5s)
*d.* Read register value and get harmonic component and fundamental voltage/current value after transition

*Harmonic Component (%) = Register Value / 163.84*

Register address 100H~1BFH

$$\text{Fundamental Current} = \frac{\text{Register Value x } 3.2656}{2^{\text{Scale}} \text{ x } 1000}$$

Register address 1C0H, 1C2H, 1C4H

$$\text{Fundamental Voltage} = \frac{\text{Register Value x } 3.2656}{2^{\text{Scale}} \text{ x } 100}$$

Register address 1C1H, 1C3H, 1C5H
For description of the related registers, please refer to datasheet.

*Example:*

Assume:

Meter ‘s nominal voltage is 220V, nominal current is 5A

The signal source outputs 10% of 5th order harmonic component for phase A voltage and 40% of 5th order harmonic for phase A current.

Register values are as follows after DFT computation engine:

[103H] = 0671H (1649)

[123H] = 19C9H (6601)

so the measured harmonic component is :

Voltage 5th order harmonic component = 1649 / 163.84 = 10.0647 (means 10.0647%)

Current 5th order harmonic component = 6601 / 163.84 = 40.2893 (means 40.2893%)

In application, the THD+N threshold for three-phase voltage and three-phase current can be configured. The M90E36A can judge whether the THD+N value is greater than the configured threshold by checking the corresponding status bits or the IRQ output signal. If the THD+N value is greater than the configured threshold, DFT computation engine can be started, and analysis and recording can be processed to the harmonic signal.

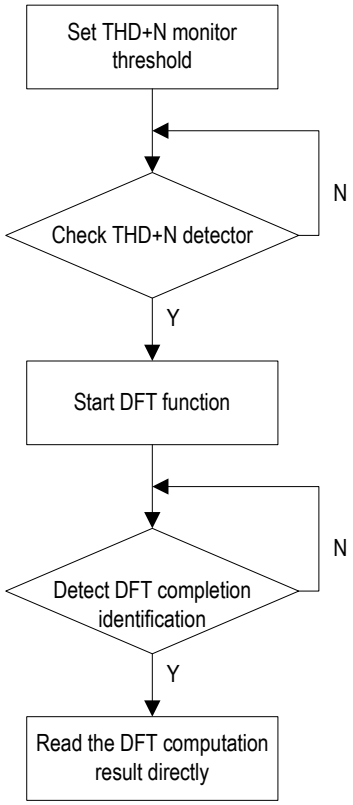



***Figure-12 Harmonic Analysis Application Flow***

## 7.2 OBTAIN HARMONIC ANALYSIS OF ABOVE 32ND

Harmonic analysis of 32nd to 42nd can be obtained as below:

1. Read the [1D7H] register (divided by 1024, current frequency can be achieved);
2. Write the value of the [1D7H] register to the 1D4H register;
3. Calculate the value of the [1D7H] register *15.872, then convert to hex. Write the high word to the [1D2H] register and the low word to the [1D3H] register;
4. Write 0x101 to the [1D1H] register to start DFT calculation;
5. Read the 33rd - 42nd order component of each phase's voltage and current in the 2nd - 11th registers when DFT calculation is complete after 0.5s (typical).

For example, if the current frequency is 50Hz, the value of the [1D7H] register is 51200 (or 0xC800). Write 0xC800 to the [1D4H] register. Meanwhile 51200*15.872=812646.4=0xC 6666, so write 0x0C to the [1D2H] register and 0x6666 to the [1D3H] register.

Of course, if not consider the influence of frequency changes to harmonic analysis, step 3 can be simplified as: write 0xC to the [1D2H] register and 0x6666 to the [1D3H] register.

It should be pointed out that because of the multiplex of some registers, the 90E36/36A can not provide harmonic analysis of the 2nd - 32nd and the 33rd - 42nd simultaneously. The common practice is to read the 2nd - 32nd harmonic analysis first, and then read the 33rd - 42nd harmonic analysis. Hence their corresponding intervals are different.

The THD data of each phase's voltage/current is analyzed based on current calculated harmonic.

2nd - 32nd harmonic analysis:

$$THD_I = \sqrt{\frac{\sum_{k=1}^{31} |X(k)|^2}{|X(0)|^2}} \times 100\%$$

33rd - 42nd harmonic analysis:

$$THD_{II} = \sqrt{\frac{\sum_{k=32}^{41} |X(k)|^2}{|X(0)|^2}} \times 100\%$$

So the THD for 2nd - 42nd order harmonic:

$$THD_T = \sqrt{THD_I^2 + THD_{II}^2}$$

# Revision History

| Doc. Rev. | Date | Comments |
|---|---|---|
| 46104A | 5/5/2014 | Initial release. |
| | | |
| | | |

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